REMARKS

Claims 1-3 are pending in the present application. Claims 1 and 3 have been amended. Claim 4 has been canceled. Applicant reserves the right to file a divisional application including canceled claim 4.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgement of the Claim of Priority Under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Claim Rejections-35 U.S.C. 103

Claims 1 and 2 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Admission) in view of the Matsumoto reference (U.S. Patent No. 5,657,330). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The microcomputer of claim 1 includes in combination among other features a test circuit "which sends a preset specific instruction to said CPU when, in said test mode, a security test signal has been output from said CPU and a specific memory area of said first and second memories has been accessed, wherein the preset specific instruction is provided from a register within said test circuit". Applicant respectfully submits that the microcomputer of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has alleged that Applicant's admitted prior art discloses all the features of claim 1, except for disclosing a security test signal output from the CPU and that a specific memory area has been accessed. In an effort to overcome these acknowledged deficiencies, the Examiner has asserted that the Matsumoto reference discloses "a security test signal has been output from said CPU and a specific memory area has been accessed. (col. 13, lines 51-58)". The Examiner has asserted that it would have been obvious to one of ordinary skill to modify the method disclosed in Applicant's admitted prior art in view of the Matsumoto reference to meet the features of claim 1.

As acknowledged by the Examiner, CPU 1 in Applicant's admitted prior art as described with respect to Fig. 2 does not output a security test signal, and test circuit 8 does not give a predetermined instruction to CPU 1 when test circuit 8 detects output of a security test signal from CPU 1 and accessing of a predetermined memory area.

As described with respect to Fig. 10 in column 13, lines 51-58 of the Matsumoto reference as relied upon by the Examiner, three-state buffers 71a – 71c output the timing signals from timers 40-42 to CPU 2. This is done during the test mode by setting the ENABLE, READ and address decode signals HIGH to turn on three-state buffers 71a – 71c. It should thus be understood that the timing signals from timers 40-42 are provided during the test mode, **irrespective of accessing of a predetermined memory area**. Particularly, accessing of memory is not described in column 13, lines 51-58 of the Matsumoto reference as relied upon by the Examiner. Storage memory is

not shown in Fig. 10 of the Matsumoto reference. Accordingly, contrary to the Examiner's assertion, the Matsumoto reference as relied upon does not disclose a test circuit that sends a preset specific instruction to a CPU during a test mode, when a security test signal is input thereto from the CPU and a specific memory area of first and second memories has been accessed.

Moreover, the prior art as relied upon by the Examiner does not disclose a test circuit which includes a register from which a preset specific instruction is provided to a CPU. The relied upon prior art thus fails to meet these further features of claim 1. Applicant therefore respectfully submits that the microcomputer of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1 and 2, is improper for at least these reasons.

Claim 3 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of the Takagi reference (U.S. Patent No. 5,280,618). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The microcomputer of claim 3 includes in combination among other features an exception processing circuit "included in said CPU, for executing a predetermined exception process responsive to a signal indicative of an unauthorized illegitimate access of said first and second memories when said functional test program is executing a security test and said memory management unit has instructed execution of

said specific operation". Applicant respectfully submits that the microcomputer of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has acknowledged that Applicant's admitted prior art as described with respect to Fig. 2 does not disclose an exception processing circuit included in CPU 1. In an effort to overcome this acknowledged deficiency, the Examiner has asserted that the Takagi reference discloses an exception processing circuit included in a CPU as described in column 2, line 51 through to column 3, line 11 and as shown in Fig. 1. The Examiner has alleged that it would have been obvious to modify the method disclosed by Applicant's admitted prior art in view of the Takagi reference to meet the features of claim 3.

The Examiner has apparently interpreted interrupt controller 9 within CPU 1 as shown in Fig. 1 of the Takagi reference as the exception processing circuit of claim 3. However, interrupt controller 9 is described very generally in column 2, line 51 through to column 3, line 11 as relied upon by the Examiner as "controlling execution of an interrupt operation of the central processing unit in response to an interrupt request signal from peripheral units". As described, the interrupt test circuit is connected between the peripheral units and the interrupt controller, and supplies a test signal to the interrupt controller within the CPU, for CPU interrupt performance tests.

Interrupt controller 9 in Fig. 1 of the Takagi reference as relied upon by the Examiner is not described as executing a predetermined exception process responsive

to a signal indicative of an unauthorized illegitimate access of first and second memories. Interrupt controller 9 is not described as executing a predetermined exception process when a functional test program is executing a security test and a memory management unit has instructed execution of a specific operation. That is, the Takagi reference as specifically relied upon is not directed to security testing to check unauthorized illegitimate access of memory. The Takagi reference as relied upon does not overcome the above noted deficiencies of Applicant's admitted prior art. Applicant therefore respectfully submits that the microcomputer of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claim 3, is improper for at least these reasons.

Conclusion

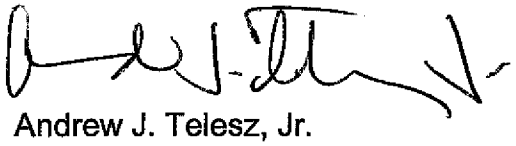
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740